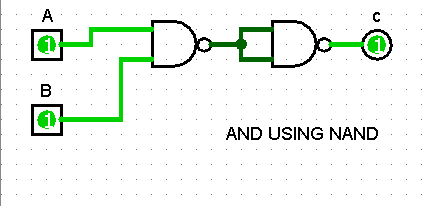
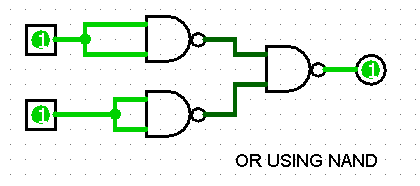
ASSIGNMENT-1

* AND gate using NAND gate

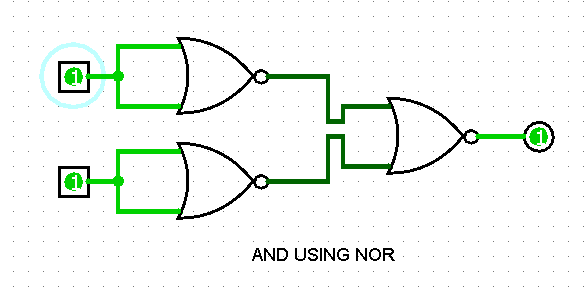
|  |  |  |
| --- | --- | --- |
| TRUTH TABLE | | |
| INPUT(A) | INPUT(B) | OUTPUT(C) |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

* OR gate using NAND gate



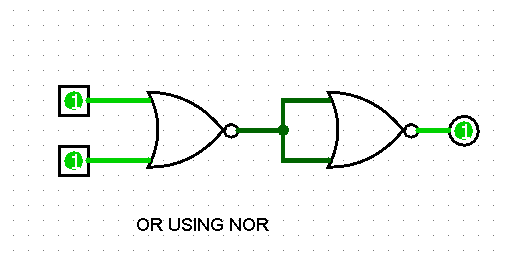
|  |  |  |
| --- | --- | --- |
| TRUTH TABLE | | |
| INPUT(A) | INPUT(B) | OUTPUT(C) |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

* AND gate NOR gate



|  |  |  |
| --- | --- | --- |
| TRUTH TABLE | | |
| INPUT(A) | INPUT(B) | OUTPUT(C) |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

* OR gate using NOR gate



|  |  |  |
| --- | --- | --- |
| TRUTH TABLE | | |
| INPUT(A) | INPUT(B) | OUTPUT(C) |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

SUBMITTED BY

YASH GUPTA

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